

Fig. 1

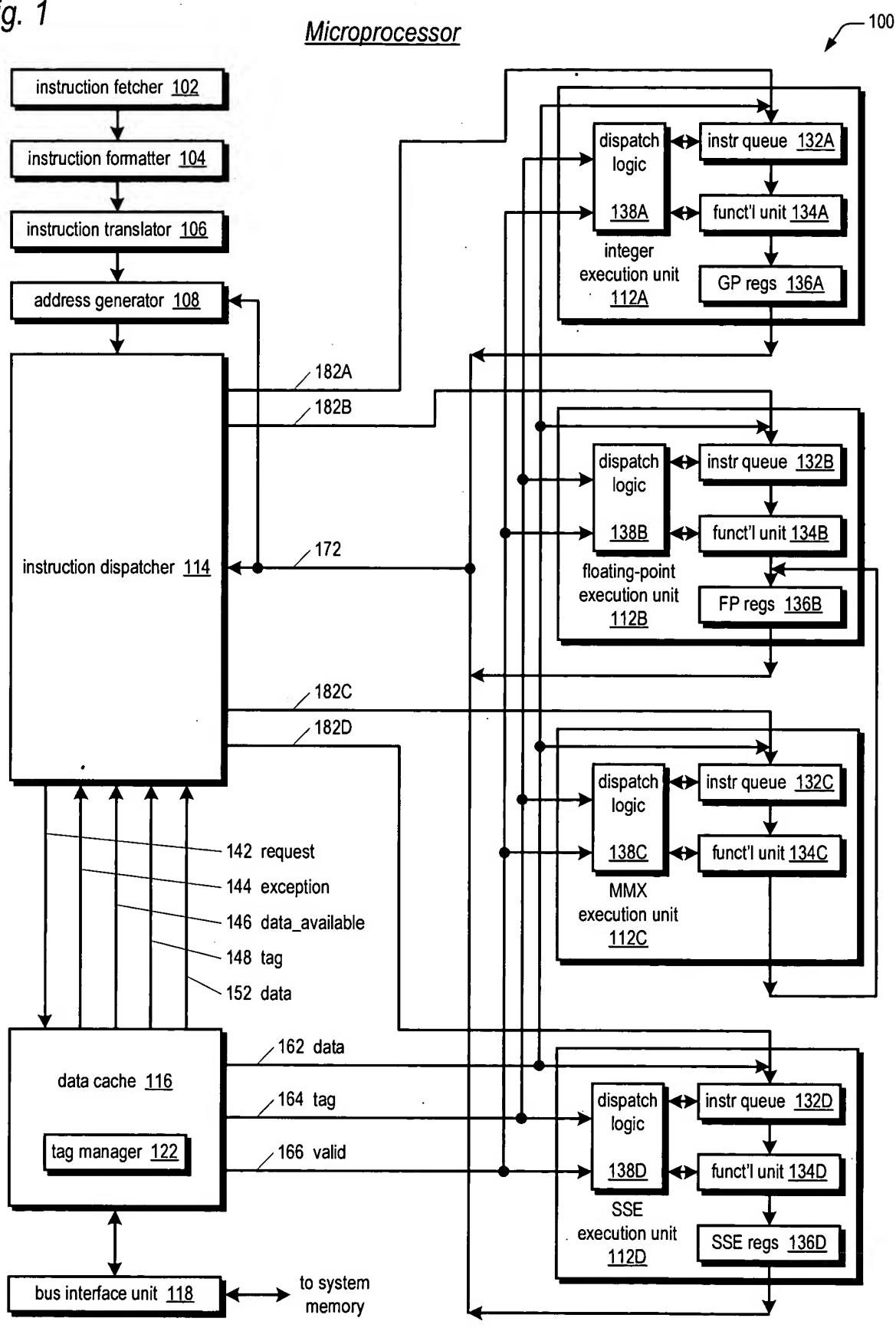
Microprocessor

Fig. 2

Instruction Queue

+ 132

data 202	DV 204	tag 206	instruction 208	IV 212
data 202	DV 204	tag 206	instruction 208	IV 212
data 202	DV 204	tag 206	instruction 208	IV 212
data 202	DV 204	tag 206	instruction 208	IV 212
data 202	DV 204	tag 206	instruction 208	IV 212
data 202	DV 204	tag 206	instruction 208	IV 212
data 202	DV 204	tag 206	instruction 208	IV 212
data 202	DV 204	tag 206	instruction 208	IV 212

222 queue entry

Fig. 3

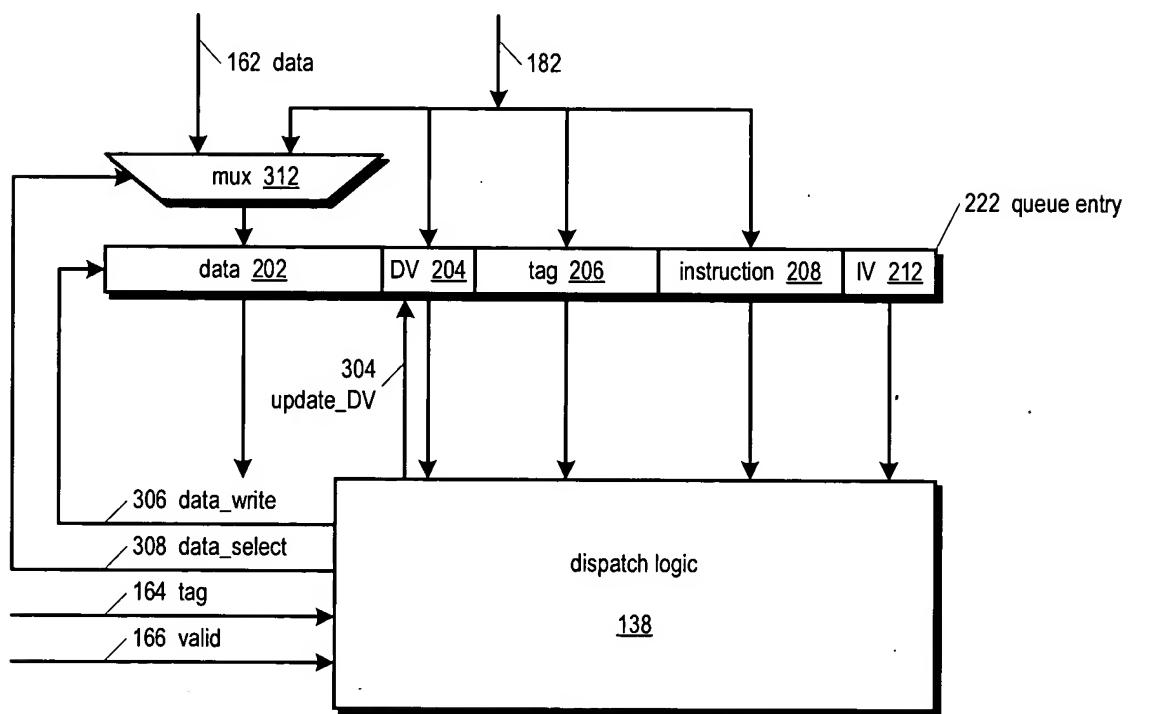
Execution Unit

Fig. 4

Detached Load Operation